REMARKS

Claims 1, 8-10, 13 and 16 have been amended. Claims 18 and 19 have been added, and claim 2 has been canceled. Claims 1 and 3-19 are pending.

Claim rejections – 35 U.S.C. 102

Claims 1-7 were rejected by the Office Action as being anticipated by Teronai et al. (JP 11-175022). Claim 1 has been amended. Amended claim 1 clarifies that the drivers are arranged in discrete groups that are located along the periphery of the chip. Memory portions are coupled to the groups and the drivers and memory portions are on the same chip. No new matter has been added. See for example, page 20, line 23 to page 21, line 4. The multiple drivers and memory portions arranged on the same chip, as recited in claim1, may enable a smaller chip size by enabling a smaller area for wiring of the memory portions to the drivers.

In contrast, Teronai et al. does not disclose discrete memory portions (plural) as recited in amended claim 1. Teronai et al. discloses a memory portion (6) (singular) connected to the anode drivers (2) and the cathode drivers (5). Further, Teronai et al. does not disclose that the drivers are arranged in discrete groups as recited in amended claim 1. In addition, the structure of Teronai et al. does not show the drivers and the memory portions made in one chip.

Teronai et al. does not teach or suggest having a plurality of discrete memory portions and drivers arranged in discrete segments on one chip. There is no suggestion that Teronai et al. recognizes that coupling the discrete memory portions with the discrete segments on one chip may reduce chip size and impedance influences by enabling reduction in area for wiring.

The present application is not anticipated by Teronai et al because the cited reference does not teach each and every limitation recited in claim 1.

Claims 3-7 depend from claim 1 and should be allowable for at least the same reasons.

Applicants respectfully request withdrawal of the 35 U.S.C. 102 rejection of claims 1 and 3-7.

Claims 8-17 were rejected by the Office Action as being anticipated by Minami et al. (USPN 6,522,003). Claim 8 has been amended to recite that the semiconductor device comprises discrete memory portions. Dependent claim 10 has been amended to remove the recitation of "memory portions" recited in amended claim 8.

Minami et al. discloses a semiconductor device having wirings formed on an interlayer insulating film. Col. 1, lines 8-12. The method helps miniaturize the device by suppressing motion of the wiring to help increase the density of the wiring on the semiconductor chip. Col. 2, lines 27-32, and col. 3, lines 47-50. The method discloses that wiring formed on the interlayer insulating film is connected to the electrically isolated pattern region via the underlying holes in the location where the wiring is not connected to the underlying wiring. Col. 3, lines 39-46.

However, Minami et al. does not disclose arranging the semiconductor output regions corresponding to one bit to constitute discrete output bit groups as recited in claim 8.

There is no hint or suggestion that Minami et al. recognizes that arranging discrete output bit groups at a periphery of the semiconductor device having discrete memory portions can reduce the semiconductor ship size.

Claim 8 is not anticipated by Minami et al because the cited reference does not teach each and every limitation recited in that claim.

Claims 9-17 depend from claim 8 and should be allowable for at least the same reasons.

Applicants respectfully request withdrawal of the 35 U.S.C. 102 rejection of claims 9-17.

Miscellaneous

Claims 18 and 19 have been added. Claim 18 recites the limitation that the memory portions are in the center of the chip. See Page 24, lines 1-10 and FIG. 13. Claim 19 recites the limitation that the wiring of the memory portions to the drivers is arranged symmetrically on the chip. See Page 21, lines 15-18 and FIG. 11A. No new matter has been added.

Claims 9 and 16 have been amended to correct errors in syntax.

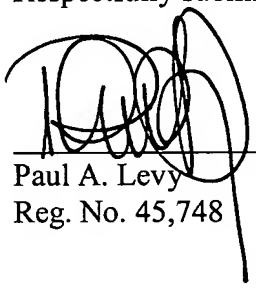
The prior art made of record has not been discussed because it has not been applied to any of the claims.

Conclusion

All pending claims are in condition for allowance.

Applicants do not believe that any charges are due. However, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,



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